Design of a Simple General-Purpose Processor

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Section 11

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**Introduction**

This lab involves the use of many components that come together to make an Arithmetic and Logic Unit. There are 2 latches which are storage units used to store the input and pass it to the other components in the circuit. The Control Unit consists of 2 separate components: the finite state machine and the 4 to 16 decoder. The finite state machine is used in the Control Unit to help determine the controller sequence. The 4 to 16 decoder is implemented to take the current output of the finite state machine and output the microcode used in the ALU component. Another component is the Arithmetic Logic Unit which takes the output of the 4 to 16 decoder and applies the operation from the microcode onto the 2 inputs from the 2 latches. The final component is the 7-segment display which takes in 4-bit data and outputs 7-bit data suitable for the input into a 7-segment display.

**Chapter 1:** Components: Latch1, Latch2, 4:16 Decoder, FSM

* 1. Latch1 and Latch2

These components temporarily store the input and pass the inputs off to the components that are connected to its output. Depending on the reset and clock inputs, the output would be determined accordingly.

A picture containing calendar

Description automatically generated

**Figure 1.1:** Truth table for latch component

A picture containing timeline

Description automatically generated

**Figure 1.2:** Example waveform of a Latch component

* 1. 4:16 Decoder

This component takes a 4-bit input and determines which one of the 16 outputs will be in a high state. This component includes subcomponents, a splitter and combiner made from scratch. These 2 components are made just so the symbol created for the final schematic would have 1 input and 1 output bus.

A picture containing wall, shelf, light

Description automatically generated

**Figure 1.3:** Truth table for 4:16 decoder

Diagram

Description automatically generated

**Figure 1.4:** Block Schematic Diagram of 4:16 decoder

Graphical user interface

Description automatically generated

**Figure 1.5:** Example waveform for 4:16 Decoder

* 1. FSM

This component takes a clock input and cycles through a set of values. A reset input is also available to reset the cycle back to the first state. This component outputs the value set at that specific state through 2 outputs, one being the current state of the finite state machine and the other being the microcode related to that state.

Diagram, table

Description automatically generated

**Figure 1.6:** State table and state assigned table for FSM

Diagram

Description automatically generated with medium confidence

**Figure 1.7:** Example waveform for finite state machine

**Chapter 2:** ALU for Problem Set 1

The purpose of the ALU is to perform a set of functions indicated in the given lab manual. The design is very basic with the each of the registers connected to a register which feed into the ALU. A clock input will be driving the control unit which would then output a set of microcode instructing the ALU on what operation to perform on the 2 inputs.

Diagram, schematic

Description automatically generated

**Figure 2.1:** Block Schematic Diagram for the General Processor Unit

The inputs of the ALU component consists of clock, A, B, and OP. The clock component controls when the component is active and when it will perform a action. A and B are the inputs which provide an 8-bit input which is then used to perform actions on by the ALU. The op input takes the microcode generated by the decoder and performs an action on the A and B inputs based on what microcode instruction it takes in. The outputs of the ALU consists of neg, r1, and r2. The neg output is responsible for driving the negative 7-seg display for r2. R1 and r2 are the outputs for 4-bits each of the ALU. R2 is responsible for displaying the first 4 bits and r1 is responsible for displaying the second 4 bits. Together, they display hexadecimal representation of the binary number result of the operation.

Table

Description automatically generated

**Figure 2.2:** Microcode generated by decoder and the functions performed by ALU given microcode

Diagram

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**Figure 2.3:** Example waveform for General Processor Unit with A input of 67 and B input of 32

**Chapter 3:** ALU for Problem Set 2

The purpose of the ALU is to perform a set of functions indicated in the given lab manual. The design is very basic with the each of the registers connected to a register which feed into the ALU. A clock input will be driving the control unit which would then output a set of microcode instructing the ALU on what operation to perform on the 2 inputs. This problem set has many different variations, I was assigned part A variation.

Diagram, schematic

Description automatically generated

**Figure 3.1:** Block Schematic Diagram for the General Processor Unit

The inputs of the ALU component consists of clock, A, B, and OP. The clock component controls when the component is active and when it will perform a action. A and B are the inputs which provide an 8-bit input which is then used to perform actions on by the ALU. The op input takes the microcode generated by the decoder and performs an action on the A and B inputs based on what microcode instruction it takes in. The outputs of the ALU consists of neg, r1, and r2. The neg output is responsible for driving the negative 7-seg display for r2. R1 and r2 are the outputs for 4-bits each of the ALU. R2 is responsible for displaying the first 4 bits and r1 is responsible for displaying the second 4 bits. Together, they display hexadecimal representation of the binary number result of the operation.

Table

Description automatically generated

**Figure 3.2:** Microcode generated by decoder and the functions performed by ALU given microcode

Calendar

Description automatically generated

**Figure 3.3:** Example waveform for General Processor Unit with A input of 67 and B input of 32

**Chapter 4:** ALU for Problem Set 3

The purpose of the ALU is to perform a set of functions indicated in the given lab manual. The design is very basic with the each of the registers connected to a register which feed into the ALU. A clock input will be driving the control unit which would then output a set of microcode instructing the ALU on what operation to perform on the 2 inputs. This problem set has many different variations, I was assigned part B variation.

Diagram, schematic

Description automatically generated

**Figure 4.1:** Block Schematic Diagram for the General Processor Unit

Table

Description automatically generated

**Figure 3.2:** Microcode generated by decoder and the functions performed by ALU given microcode

Calendar

Description automatically generated with medium confidence

**Figure 4.3:** Example waveform for General Processor Unit with r1 and r2 displaying y or n

**Conclusion**

In conclusion, it can be understood from this lab that the ALU is a component that can handle many inputs and decide based off microcode, what action it’ll perform. A simple control unit can be studied with this lab as the components inside the control unit show how a clock signal can be used to drive components capable of outputting instructions. Latches were also used in this lab which can help students learn the capabilities of an SR-latch and how it is able to temporarily store the input as well as passing it on with the correct high signals.